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PTO/SB/21 (08-00)

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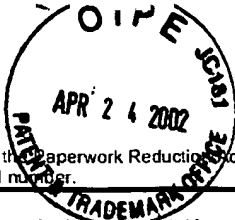
TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/759,414
	Filing Date	01-13-2001
	First Named Inventor	LI, ZHE
	Group Art Unit	2123
	Examiner Name	TESKA, KEVIN J
Total Number of Pages in This Submission	Attorney Docket Number	

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		Applicant Number	09/759,414
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	01-13-2001
		First Named Inventor	LI, ZHE
		Group Art Unit	2123
		Examiner Name	TESKA, KEVIN J
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Sheet	1	of	2

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		S.-Y. HUANG et al, "AutoFix: a hybrid tool for automatic logic rectification" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1376-1384, IEEE, U.S.A.	
		S.-Y. HUANG and K.-T. CHENG, "ErrorTracer: design error diagnosis based on fault simulation techniques" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1341-1352.	
		C.-C. LIN et al, "Logic synthesis for engineering change" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 3, March 1999, pp. 282-292, IEEE, U.S.A.	
		S.-Y. HUANG et al, "Fault simulation based design error diagnosis for sequential circuits" Proceedings Design Automation Conference, June 1998, pp. 632-637, ACM, U.S.A.	
		A. G. VENERIS and I.N. HAJJ, "A fast algorithm for locating and correcting simple design errors in VLSI digital circuits" Proceedings Great Lake Symposium on VLSI Design, March 1997, pp. 45-50, IEEE, U.S.A.	
		S.-Y. HUANG et al, "Incremental logic rectification" Proceedings VLSI Test Symposium, April 1997, pp. 143-139, IEEE, U.S.A.	
		S.-Y. HUANG et al, "ErrorTracer: a fault simulation-based approach to design error diagnosis" Proceedings International Test Conference, November 1997, pp. 974-981, IEEE, U.S.A.	
		C.-C. LIN et al, "Logic synthesis for engineering change" Proceedings Design Automation Conference, June 1995, pp. 647-652, ACM, U.S.A.	
		I. POMERANZ and S. REDDY, "On correction of multiple design errors" IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 2, February 1995, pp. 255-264, IEEE U.S.A.	
		I. POMERANZ and S. M. REDDY, "On error correction in macro-based circuits" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 568-574, ACM, U.S.A.	
		D. BRAND et al, "Incremental synthesis" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 14-18, ACM, U.S.A.	

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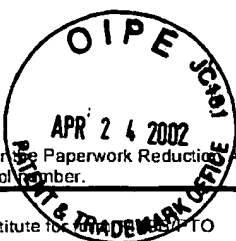
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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		A. KUEHLMANN et al, "Error diagnosis for transistor-level verification" Proceedings Design Automation Conference, June 1994, pp. 218-224, ACM, U.S.A.	
		I. POMERANZ and S.M. REDDY, "A method for diagnosing implementations errors in synchronous sequential circuits and its implications on synthesis" Proceedings European Conference on Design Automation, September 1993, pp. 252-258, IEEE.	
		M. FUJITA, "Methods for automatic design error correction in sequential circuits" Proceedings European Conference on Design Automation, September 1993, pp. 76-80, IEEE.	
		P.-Y. CHUNG et al, "Diagnosis and correction of logic design errors in digital circuits" Proceedings Design Automation Conference, June 1993, pp. 503-508, IEEE, U.S.A.	
		S.-Y. KUO, "Locating logic design errors via test generation and don't-care propagation" Proceedings European Design Automation Conference, September 1992, pp. 466-471, IEEE.	
		P.-Y. CHUNG and I.N. HAJJ, "ACCORD: automatic catching and correction of logic design errors in combinational circuits" Proceedings International Test Conference, October 1992, pp. 742-751, IEEE, U.S.A.	
		Y. WATANABE and R. BRAYTON, "Incremental synthesis for engineering changes" Proceedings International Conference on Computer-Aided Design, November 1991, pp. 40-43, IEEE, U.S.A.	
		M. TOMITA et al, "An algorithm for locating logic design errors" Proceedings International Conference on Computer-Aided Design, November 1990, pp. 468-471, IEEE, U.S.A.	
		H.-T. LIAW et al, "Efficient automatic diagnosis of digital circuits" Proceedings International Conference on Computer-Aided Design, November 1990, pp. 464-467, IEEE, U.S.A.	
		J.C. MADRE et al, "Automating the diagnosis and the rectification of design errors with PRIAM" Proceedings International Conference on Computer-Aided Design, November 1989, pp. 30-33, IEEE, U.S.A.	
		K.A. TAMURA, "Locating functional errors in logic circuits" Proceedings Design Automation Conference, June 1989, pp. 185-191, ACM, U.S.A.	

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